

Form PTO-1449 Modified List of Patent and Publications Cited by Applicant (Use several sheets if necessary) U.S. Department of Commerce Patent and Trademark Office	Docket No. MSFT-2865 / 304048.02	Application No. 10/777,797
	Applicant Steve Pronovost, Anuj B. Gosalia, Byran L. Langley and Hideyuki Nagase	
	Filing Date February 12, 2004	Group 2182
	Confirmation No. 5844	

U. S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass
	1	5,777,629	07/07/98	Baldwin	345	506
	2	5,896,141	04/20/99	Blaho et al.	345	541
	3	5,918,050	06/29/99	Rosenthal et al.	718	108
	4	6,023,738	02/08/00	Priem et al.	710	23
	5	6,049,857	04/11/00	Watkins	711	207
	6	6,065,071	05/16/00	Priem et al.	710	22
	7	6,252,600	06/26/01	Kohli et al.	345	219
	8	6,437,788	08/20/02	Milot et al.	345	552
	9	6,446,186	09/03/02	Priem et al.	711	206
	10	6,518,973	02/11/03	Blythe	345	564
	11	6691180	02/10/04	Priem et al.	710	23

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Country	Translation	
					YES	NO
	12	WO 02/09083	01/31/02	PCT		

EXAMINER	DATE CONSIDERED
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NON-PATENT DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
	13	Intel Corp, "Accelerated Graphics Port Interface Specification, Revision 1.0," July 1996 , 1-161	
	14	Martin, K.E. et al., "Direct Rendering Infrastructure, Low-Level Design Document," http://dri.sourceforge.net/doc/design_low_level.html , May 1999 , 1-18	
	15	Owen, J. et al., "A Multiple Direct Rendering Architecture for 3D," http://dri.sourceforge.net/doc/design_high_level.html , September 1998 , 1-10	

EXAMINER	DATE CONSIDERED
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